

(19)



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Office européen des brevets



(11)

EP 1 014 582 A1

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
28.06.2000 Bulletin 2000/26

(51) Int Cl.⁷: H03K 19/003, H03K 19/0175,
G06F 13/40

(21) Application number: 99309742.7

(22) Date of filing: 03.12.1999

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU
MC NL PT SE
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: 09.12.1998 US 207255

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(54) Digital signal transmitter and receiver using source based reference logic levels

(57) A signal transmitter for transmitting digital logic signals and a complementary receiver, are disclosed. The signal transmitter comprises a plurality of signal drivers and at least one reference driver. The signal drivers transmit digital signals, while the reference driver transmits a constant signal representative of a digital HI or LO. The signal and reference drivers are interconnected so that any noise due to package and power supply interconnection impedances is present in all transmitted signals including any reference signals. At a receiver, the reference signal including noise is used to establish threshold levels for digital HI and LO signals. Because noise is common to all transmitted signals, the receiver is able to reduce the effects of the noise by comparing the plurality of received signals with the reference signal.

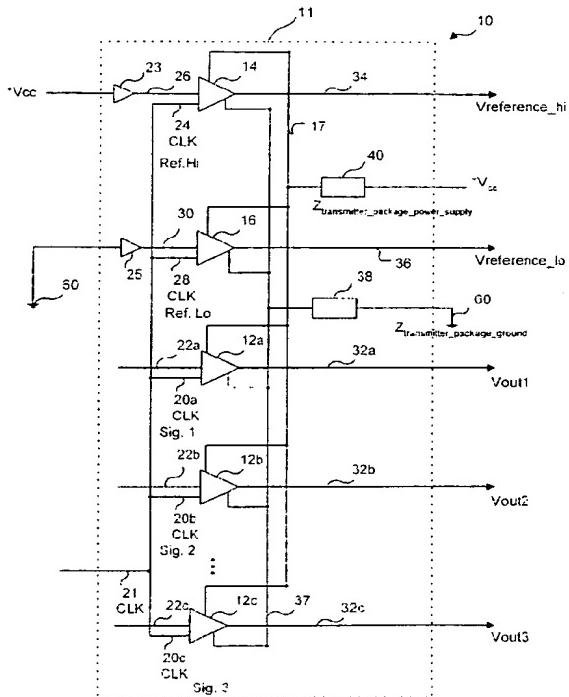


FIG. 1

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Description**FIELD OF THE INVENTION:**

- 5 [0001] The present invention relates to a signal transmitter for transmitting digital logic signals and a complementary receiver, and more particularly to a digital logic transmitter that generates one or more reference signals, to be used by the receiver to establish threshold levels for digital HI and LO signals.

BACKGROUND OF THE INVENTION:

10 [0002] Digital electronic systems typically utilize very large scale integrated circuit ("VLSI") blocks. VLSI blocks are interconnected to each other within an electronic system by electronic conductors that act as transmission lines. Digital HI and LO signals are represented by two distinct voltage levels presented on the conductors. A "driver" forming part of one VLSI block couples a transmitting VLSI block to the transmission lines. Similarly, a "receiver", forming part of a receiving VLSI block, couples the receiving VLSI block to the lines. Each driver and receiver typically comprises a plurality of transistors formed on the respective VLSI blocks.

15 [0003] The transistors forming the drivers and receivers are coupled to ground points on the VLSI blocks. These ground points, however, are not at the same potential as the external ground potential of the VLSI packages. Drivers are coupled to the external ground connection through a package impedance. This package impedance typically has resistive, inductive, and capacitive components and is therefore a source of electrical noise present when a driver receives switches from LO to HI or HI to LO. This noise is typically referred to as a "ground bounce".

20 [0004] At the receiver, binary HI and LO signals are typically distinguished by their voltage levels relative to the receiver package ground. Signals that exceed a threshold voltage level represent a digital HI while signals that fall beneath another threshold voltage represent a digital LO. As will be appreciated, the presence of noise from the transmission signal at the transmitter, may cause a signal not intended to cross a threshold to cross this threshold, as

25 [0005] Numerous digital drivers and receivers address this problem. For example, the gunning transceiver logic ("GTL") family as more particularly described in U.S. Patent No. 5,023,488 uses low voltage swings that reduce transient effects of parasitic impedances, including package impedances. As well, this patent discloses clamping the drain to

30 source of a GTL driver to reduce the rate at which current is drawn so as to provide increased damping for noise due to transient voltages.

[0006] Still other logic families use differential outputs. As the effect of parasitic impedances is the same for both outputs of a differential pair, differential signals naturally reject common mode noise. Differential signals, however, require double the number of outputs for a transmitting VLSI block; double the number of transmission lines interconnecting the transmitting VLSI block to the receiving VLSI block; and double the number of inputs at the receiving VLSI block. As will be appreciated, it would often be desirable to eliminate these extra inputs, outputs and interconnects.

[0007] Accordingly, an alternative to known approaches to reduce the effects of package impedance in digital transmitters and receivers is desirable.

SUMMARY OF THE INVENTION:

40 [0008] In accordance with the present invention a transmitter and complementary receiver use HI and/or LO reference signals generated at the transmitter, and transmitted to the receiver. The reference signals are used at the receiver to account for noise components in received signals that are representative of digital HI or LO signals.

45 [0009] In accordance with an aspect of the invention, there is provided a signal transmitter block formed as part of an integrated circuit. The transmitter block transmits digital signals to a receiver. The transmitter block includes several signal drivers, each for generating output voltages at a signal driver output, that when measured relative to a ground point on the integrated circuit are representative of digital HI and LO signals. A first reference driver, for generating at a first reference output an output voltage that when measured relative to the ground point, corresponds either a digital HI signal; or a digital LO signal, forms part of the block. The first reference driver and the signal drivers are electrically interconnected to the ground point on the integrated circuit block. The ground point is further interconnected through an impedance on the integrated circuit block to a system ground connection for the integrated circuit, so that current flowing from and to the system ground connection through the ground point to the signal drivers and the first reference driver flows through the impedance.

50 [0010] In accordance with another aspect of the invention, a digital signal receiver block having receiver block outputs for generating digital HI and LO signals, includes several comparators. Each comparator has a signal input for receiving a voltage signal representative of one of a digital HI signal and LO signal and a noise signal; an output interconnected with one of the receiver block outputs; and a first reference input for receiving a reference voltage signal including a

signal indicative of a digital LO signal, and a noise signal. The first reference inputs of the several comparators are interconnected so that each of the reference inputs receives the same reference voltage signal. Each of the comparators is adapted to produce at its output a signal representative of a digital LO signal when a voltage at its signal input is less than a threshold voltage derived from a reference voltage at its first reference input.

[0011] In accordance with yet another aspect of the present invention, there is provided a method of transmitting and receiving several signals representative of digital HI and LO signals from a transmitter to a receiver. The method includes the steps of a. concurrently transmitting the several signals, each having a voltage level representative of one of a digital HI and LO signal and a noise signal from a transmitter to a receiver; b. transmitting a reference signal comprised of a signal having a voltage level representative of a HI signal and a noise signal to the receiver; c. receiving the several signals and the reference signal at the receiver; d. comparing the reference signal to each of the several signals; e. outputting a signal representative of a digital HI signal at the receiver, for each of the several signals that exceeds a threshold voltage derived from the reference signal.

[0012] Advantageously, the invention provides rejection of noise signals without the use of differential signals.

[0013] Other aspects and features of the present invention will become apparent to those of ordinary skill in the art upon review of the following description of specific embodiments of the invention in conjunction with the accompanying figures.

BRIEF DESCRIPTION OF THE DRAWING:

[0014] In figures which illustrate, by way of example only, embodiments of the present invention,

FIG. 1 is a schematic diagram of a digital transmitter block exemplary of an embodiment of the present invention;
 FIG. 2 is a schematic diagram of a receiver block exemplary of an embodiment of the present invention
 FIG. 3 is a schematic diagram of a signal transmitter and receiver system exemplary of an embodiment of the present invention;
 FIG. 4 illustrates a plurality of signal waveforms present in the system of FIG.3, in operation; and
 FIG. 5 illustrates a further plurality of signal waveforms, present in the system of FIG. 3, in operation.

DETAILED DESCRIPTION:

[0015] FIG.1 schematically illustrates a signal transmitter block 10, exemplary of a preferred embodiment of the present invention. Signal transmitter block 10 is formed as part of a VLSI block 11 in accordance with generally known VLSI design and fabrication techniques.

[0016] Transmitter block 10 comprises a plurality of digital signal drivers 12a to 12c (individually and collectively 12). For clarity, only three signal drivers are illustrated. A person skilled in the art will appreciate that a typical transmitter (usually comprises) more than three drivers. Each driver has a signal input 22 (22a to 22c for drivers 12a to 12c, respectively); a clock input 20 (20a to 20c for drivers 12a to 12c, respectively); and an output 32 (32a to 32c for drivers 12a to 12c, respectively). On the transition of a clock pulse at clock input 20, a driver presents at its output 32 voltage levels representative of digital HI and LO signals corresponding to an input signal presented at its signal input 22.

[0017] Transmitter block 10 further comprises a reference HI driver 14 and reference LO driver 16, having signal inputs 26 and 30, clock inputs 24 and 28, and outputs 34 and 36, respectively. Like signal drivers 12, reference drivers 14 and 16 present at their outputs 34 and 36 signals representative of their inputs 26 and 30 upon the transition of a clock signal at clock inputs 24 and 28.

[0018] Preferably, a common clock input 21, interconnects all clock inputs 20, 24 and 28 of drivers 12, 14 and 16.

[0019] All of the drivers 12, 14 and 16 are preferably formed of identical electric components and typically comprise one or more known transistor devices. Each driver may for example be a CMOS or bi-polar driver providing transistor to transistor (TTL) logic, positive emitter coupled logic (PECL), or other outputs. A person skilled in the art will appreciate that other drivers may be appropriately used. Reference drivers 14 and 16 are thus typical drivers, of the same type used as signal drivers 12.

[0020] As illustrated, each driver 12, 14, 16 is connected to a positive voltage source rail 17 interconnected through power supply interconnection impedance $Z_{\text{transmitter-package-power-supply}}$ 40 to external power supply voltage $+V_{cc}$. Further, each driver is connected to an on chip ground rail 37 (GND) formed as part of VLSI block 11. VLSI block 11 is further connected to an external system ground 60. Because of the package impedance of VLSI block 11 and system ground impedances unique to the transmitter ground current path, ground rail 37, the ground connection point for drivers 12, 14 and 16, is actually coupled to system ground 60 through an impedance that may modelled by an impedance $Z_{\text{transmitter-package-ground}}$ 38. The combination of impedances $Z_{\text{transmitter-package-power-supply}}$ 40 and $Z_{\text{transmitter-package-ground}}$ 38 represent the total package impedance of VLSI block 11. Power supply interconnection impedance $Z_{\text{transmitter-package-power-supply}}$ 40 and ground impedance $Z_{\text{transmitter-package-ground}}$ 38 may be modelled as having resistive, capacitive and inductive components. As will be

appreciated, it is possible that power supply interconnection impedance $Z_{\text{transmitter-package-power-supply}}$ 40 and package impedance $Z_{\text{transmitter-package-ground}}$ 38 are non-linear.

[0021] Signal inputs 26 and 30 of reference drivers 14 and 16 are interconnected with gates 23 and 25, respectively. The input of gate 23 is connected to $+V_{cc}$ causing the output of gate 23 to produce a voltage representative of a logic HI at input 26 of driver 14. Similarly, the input of gate 25 is connected to system ground 60 causing the output of gate 25 to produce a voltage representative of a logic LO signal at input 30 to driver 16. As will become apparent, outputs 34 and 36 of drivers 14 and 16 thus always generate HI and LO output signals, used as reference signals. Gates 23 and 25 need not be formed as part of transmitter block 10.

[0022] Signal inputs 22 to drivers 12 may be interconnected to n input signals, typically originating on VLSI block 11. These input signals may, for example, ultimately emanate from n address or data lines of an n bit computer bus. Typically, these n input signals are synchronous and clocked by their source. Common clock input 21 is thus typically interconnected to a system clock which may also be provided by the clock of a computer.

[0023] FIG. 2 illustrates a receiver block generally marked 70 exemplary of a preferred embodiment of the present invention. In the preferred embodiment, receiver block 70 is formed as part of a VLSI block 72 that is physically distinct from VLSI block 11 (FIG. 1). VLSI block 72 is connected to system ground 90. Receiver block 70 comprises a plurality of comparators 74a to 74c (individually and collectively 74). For clarity, only three comparators 74a to 74c are illustrated. A person skilled in the art will appreciate that a typical receiver block comprises more than three such comparators and typically one comparator for each transmitter in a complementary transmitter block. Each comparator 74 takes at its input 80 (80a to 80c for comparators 74a to 74c, respectively) a reference signal and an input signal at input 78 (78a to 78c for comparators 74a to 74c, respectively). Outputs 82 (82a to 82c for comparators 74a to 74c, respectively) present a fixed output voltage if an associated input 78 is less than a trigger voltage derived from the reference signal at reference input 80. Typically, the trigger voltage equals the reference voltage plus a noise or hysteresis margin, V_{margin} . Comparators 74 may be designed to allow for adjustment to the hysteresis margin, in accordance with design techniques known to those skilled in the art.

[0024] As illustrated, each comparator 74 is connected to a positive voltage source $+V_{cc}$, preferably interconnected with $+V_{cc}$ of VLSI block 11. Package and power supply interconnect impedances of VLSI block 70 that might be modelled similar to $Z_{\text{transmitter-package-ground}}$ 38 and $Z_{\text{transmitter-package-power-supply}}$ 40 of VLSI block 11 have been illustrated as $Z_{\text{receiver-package-ground}}$ 66 and $Z_{\text{receiver-power-supply}}$ 68.

[0025] Outputs 82 of comparators 74 are interconnected with latching block 76. Latching block 76 further takes as an input a clock signal presented at clock input 84. Latching block 76 latches at its outputs 86a to 86c (individually and collectively 86) logic input values 82a to 82c, respectively, upon sensing a transition of clock input 84. Latching block 76 may for example comprise a plurality of D-type flip-flops whose inputs are connected to comparator outputs 82a to 82c and whose outputs represent the latch outputs 86a to 86c. A person skilled in the art will appreciate a variety of latching circuits that could be used in place of the D-type flip flops. Typically, outputs 86 are interconnected with another functional circuit block (not shown) of VLSI block 72, that may process signals presented at outputs 86.

[0026] FIG. 3 illustrates an exemplary interconnection of transmitter block 10 (FIG. 1) with receiver block 70 (FIG. 2) forming a digital transmitter and receiver system generally marked 92. As illustrated outputs 34 and 32a to 32c of transmitter block 10 are interconnected with transmission lines 94, and 96a to 96c, respectively. Ground 60 is interconnected with ground 90. These transmission lines are typically traces of a printed circuit board interconnecting VLSI blocks 11 and 72.

[0027] Inputs 78a to 78c of receiver block 70 are interconnected with the terminating ends of transmission lines 96a to 96c. Additionally, transmission line 94 interconnected with reference HI driver 14, is interconnected with reference input 80a (80 in FIG. 3) of receiver block 70. As well, a common clock source is interconnected with driver clock input 21 and receiver block clock input 84. Of course, clock input 84 could be driven by a signal otherwise derived and interrelated with a signal at clock input 21. For example, VLSI block 72 could comprise a phase locked loop, locked to a clock signal on VLSI block 11 used to clock receiver block 70.

Alternatively, a clock signal may be recovered from a data stream at receiver block 70.

[0028] In system 92, reference HI driver 14 and its output 34 are not interconnected to receiver block 70. As will become apparent, reference drivers 14 and 16 provide voltage levels representative of digital reference HI and LO signals, respectively. Only one of reference drivers 14 or 16 is required. Thus, one of drivers 14 and 16 is optional and could be eliminated. In practise, if only a single reference driver is used, reference LO driver 14 is preferably used as "ground bounce" noise more significantly affects logic LO signals, than logic HI signals.

[0029] FIGS. 4 and 5 illustrate various signals present in the system depicted in FIG. 3, in operation.

[0030] Specifically, FIG. 4 illustrates input signals present at transmitter block 10 for two complete clock cycles 100 at clock inputs 21 and 84 as shown in FIGS. 1-3.

[0031] In the operational example, voltage levels representing digital HI and LO signals are represented by positive voltage values $+V_{cc}$ for binary HI signals and $.7+V_{cc}$ for binary LO signals, both measured relative to system ground 60. The receiver is designed to operate with a hysteresis or noise margin of $.1+V_{cc}$. Accordingly, a binary HI signal is

therefore generated for inputs greater than $.9V_{cc}$, while a binary LO signal is generated for inputs less than $.8V_{cc}$. In other words, voltage signals exceeding $.9V_{cc}$ are interpreted as digital HI signals, while voltage signals less than $.8V_{cc}$ are interpreted as digital LO signals. Of course, depending on the precise drivers, transmitters and receivers exemplary of the present invention may use other voltage levels, such as for example, typical CMOS or TTL logic levels.

[0032] In the illustrated example, signals 106 and 108 are applied to signal inputs 22a and 22b, of drivers 12a and 12b of transmitter block 11 (FIGS. 1 and 3), respectively. As illustrated input signal 106 represents a binary HI in both clock cycles, while input signal 108 represents a binary HI signal in a first clock cycle, followed by a transition to a binary LO in a second clock cycle. For illustration, voltages representing logic HI and LO values at inputs 22 are chosen as $+V_{cc}$ and $.7V_{cc}$, respectively. Of course, logic voltage levels at inputs 22 need not be related to output voltages or threshold voltages presented at inputs 26 and 30. Transmitter block 10 could easily be adapted to translate input logic levels to other output values. Signals 100, 102, 104 and 106 are measured relative to GND at rail 37, and are therefore free from noise due to the package impedance $Z_{transmitter_package_ground}$ 38 and $Z_{transmitter_package_power_supply}$ 40 of VLSI block 11.

[0033] The outputs of transmitter block 10, at outputs 34, 36 and 32a and 32b (illustrated in FIG. 1) measured relative to system ground 60, in operation, are depicted in FIG. 5. As well, for convenience, clock signal 100 is again illustrated.

[0034] As illustrated, $V_{reference_hi}$ and $V_{reference_lo}$ deviate from the expected $+V_{cc}$ and $+.7V_{cc}$ because of the voltage drops across $Z_{transmitter_package_ground}$ 38 and $Z_{transmitter_package_power_supply}$ 40.

[0035] Output reference signal $V_{reference_hi}$ 110 measured relative to system ground 60 at output 34 of driver 14 exhibits slight ringing (not shown) at the commencement of each cycle of clock signal 100. This ringing is attributable to transient current through package impedance $Z_{transmitter_package_ground}$ 38 and $Z_{transmitter_package_power_supply}$ 40, and the resulting voltage signals. As previously noted, $Z_{transmitter_package_ground}$ 38 and $Z_{transmitter_package_power_supply}$ 40 may be modelled as comprising resistive, inductive and capacitive components. As illustrated, the duration of the ringing is typically only a fraction of the clock period. The duration and amplitude of the ringing is dependent on the values of $Z_{transmitter_package_ground}$ 38 and $Z_{transmitter_package_power_supply}$ 40 as well as the amount and rate of current provided to drivers 12, 14 and 16.

[0036] More significantly, as illustrated, output reference signal $V_{reference_hi}$ exhibits an upward voltage drift relative to system ground 60 at the commencement of each clock cycle. This upward drift is attributable largely to the $Z_{package_power_supply_ground}$ 38 portion of the package impedance. Specifically, as reference hi driver 14 produces its output relative to chip ground 37, and $Z_{package_power_supply_ground}$ 38 introduces a further voltage drop between chip ground 37 and system ground 60, that manifests itself in the illustrated upward drift or "ground bounce". As well, a voltage drop in the HI signals may be attributable to the voltage drop caused by current through $Z_{transmitter_package_power_supply}$ 40. However, $V_{reference_hi}$ is affected by a similar drop.

[0037] It is worth noting that effect of V_{ground_noise} is far more significant in sensing logic LO signals at the receiver. This is because the upward voltage drift caused by the voltage drop across $Z_{power_supply_ground}$ causes LO signals to drift above the threshold required by receiver 70 to detect a logic LO signal. This same drift will cause HI signals that already exceed the minimum voltage for a HI signal to merely further exceed this signal.

[0038] As such, in practise, if only a single reference driver is used, reference LO driver 14 is preferably used as "ground bounce" noise more significantly affects logic LO signals than logic HI signals.

[0039] A reference LO signal $V_{reference_lo}$ 112 at output 36 measured relative to system ground 60 experiences similar drift and ringing as do driver output signals V_{out1} 114 and V_{out2} 116 at outputs 32a and 32b of drivers 12a and 12b. As will be appreciated, and as illustrated, neglecting any pin impedance, the ringing and drift in signals 110, 112, 114 and 116 attributable to package impedance $Z_{transmitter_package_ground}$ 38 will be substantially similar in all n drivers 12a to 12c as well as reference LO and HI drivers 14 and 16 as they are connected to system ground 60 through common package impedance $Z_{transmitter_package_ground}$ 38.

[0040] Similarly, the ringing and drift in signals 110, 112, 114 and 116 attributable to power supply interconnect impedance $Z_{transmitter_package_power_supply}$ 40 will be identical, as current provided by an external power supply to all drivers 12a to 12c as well as reference LO and HI drivers 14 and 16 must flow through common power supply impedance $Z_{transmitter_package_power_supply}$ 40.

[0041] More specifically, the instantaneous output voltage of each driver at outputs 32, 34 or 36 relative to system ground 60, may be modelled as:

$$V_{out_n} = V_{driver_n} + V_{noise},$$

[0042] where V_{driver_n} is the output of the nth driver at transmitter 10, measured relative to "chip" ground 37.

[0042] Assuming that noise other than package ground and power supply interconnect noise is negligible, and further assuming that $V_{ground_noise} \gg V_{power_supply_noise}$

$$V_{out_n} = V_{driver_n} + V_{ground\ noise}$$

5 $V_{ground\ noise}$ may further be modelled as

$$V_{ground\ noise} = I_{ground\ package} * Z_{transmitter_package_ground}.$$

10 with

$$\begin{aligned} I_{ground\ package} &= I_{ground\ driver\ total} = I_{ground\ driver_1} + I_{ground\ driver_2} + \dots + I_{ground\ driver_n} \\ &\quad + I_{ground\ refdriver_hi} + I_{ground\ refdriver_lo} \end{aligned}$$

15 [0043] Thus, the instantaneous contribution of V_{noise} to each output signal V_{out_n} is identical for each driver output signal. Moreover, the contribution of V_{noise} depends on the total current drawn by transmitter block 10, and therefore will vary from clock cycle to clock cycle, depending on the number of drivers producing HI or LO outputs.

20 [0044] Assuming pin and transmission line effects are negligible, in FIG 3, signals at outputs 32a and 32b of transmitter block 10 are presented at receiver inputs 78a and 78b through lines 96a and 96b. Similarly, signal 112 of FIG. 4 at reference LO output 36 of transmitter block 10 is presented at reference LO input 80 interconnected with comparator reference inputs 80a and 80b of FIG. 2 of receiver 70 through line 94.

25 [0045] At the receiver, the effect of current drawn by the transmitter block 10 will have a negligible effect on receiver block 72. However, as illustrated, voltage levels received at the receiver block 72, measured relative to system ground 60 will fluctuate, often significantly, depending largely on the current drawn through $Z_{transmitter_package_ground}$.

30 [0046] As will become apparent, use of comparators and reference signals $V_{reference_hi}$ and $V_{reference_lo}$ signals attempt to compensate for such fluctuations.

35 [0047] Specifically the output 82 of each comparator 74 in FIG. 2, varies depending on whether or not the voltage level of the input signal at input 78 exceeds the reference voltage presented at input 80 less a hysteresis margin. If it does, output 82 will assume a voltage value representative of a digital HI signal at its output and at the input latching block 76.

40 [0048] Voltages at comparator inputs 80 and 78 are measured relative to each other. Output 82 is only LO if $V_{comparator_n} = V_{out_n} - V_{reference_lo} + V_{margin}$. Because the comparator inputs are measured relative to each other, any common mode noise in the driver and reference signal will be ignored. This is best illustrated by considering signal $V_{reference_lo}$ and V_{out} relative to system ground 60.

45 [0049] Thus,

$$V_{reference_lo} = V_{ref} + V_{noise},$$

40 where V_{ref} is the threshold voltage measured relative to chip ground rail 37 and

$$V_{comparator_n} = V_{out_n} = V_{driver_n} + V_{noise}.$$

45 [0050] As noted, this leads to a LO comparator output only when

$$V_{comparator_n} < V_{reference_lo} + V_{margin}$$

50 $V_{driver_n} + V_{noise} < V_{ref} + V_{noise} + V_{margin};$

55 or

$$V_{driver_n} < V_{ref} + V_{margin}.$$

[0051] This precisely defines the required threshold level required to generate a digital output LO signal. Thus, the parasitic effects of source package impedance $Z_{transmitter_package_ground}$ 38 and power supply interconnect impedance $Z_{transmitter_package_power_supply}$ 40, are eliminated through the use of a reference signal provided by driver 16 of transmitter block 10 to a receiver block 70 comprising a plurality of comparators 74.

5 [0052] In FIG. 2, on the rising edge of clock signal 100 of FIG. 4, latching block 76 latches at its outputs 86 the outputs of comparators 74. These outputs are typically provided to another functional block (not illustrated) formed as part of VLSI block 72.

10 [0053] Provided that drivers 12, 14 and 16 are formed in geometric proximity to each other, the effect of the package impedance $Z_{transmitter_package_ground}$ 38 on each of the drivers should be very similar if not identical, as any current passing from drivers 12, 14 and 16 to system ground 60 will flow through impedance $Z_{transmitter_package_ground}$ 38. Preferably, the location of reference drivers 14 and 16 is chosen to be near the geometric centre of interrelated drivers in a block of drivers on a VLSI block. As the number of drivers increases, and their geometric proximity decreases, the effects of package impedance on signals produced by each of the drivers will vary. It may accordingly be desirable to limit the transmitter block size, and therefore provide a single reference hi driver for a small number of drivers (ie. four, eight or sixteen drivers). Other block sizes anywhere between zero and twenty five might be appropriate. A signal transmitter may thus comprise a number of transmitter blocks substantially identical to transmitter block 10, as illustrated.

15 [0054] Alternatively, or additionally, $V_{reference_hi}$ at output 34 may be transmitted to receiver block 70 in addition to or instead of $V_{reference_lo}$ at output 36. High threshold comparisons may then be made at the receiver when

20

$$V_{out} > V_{reference_hi} - V_{margin}$$

at receiver 70.

25 [0055] This second verification allows the receiver to detect critical errors. That is, when a detected signal neither exceeds $V_{reference_hi} - V_{margin}$ nor is less than $V_{reference_lo} + V_{margin}$ an indeterminate error could be detected. Such error could be detected by other hardware blocks or, alternatively, comparators 74 could be adapted to detect such errors. The detection of such errors could be used to signal a possible hardware fault requiring signal retransmission or other error handling, or diagnosis or repair.

30 [0056] As will be appreciated, use of source side reference signals allows dynamic comparison of transmitted signals to the reference signal, which provides particular benefit for high frequency signals, for which the effects of package and power supply impedances may be particularly pronounced.

[0057] As should now also be appreciated, as reference drivers 14 and 16 should be conventional drivers, identical to signal drivers 12 existing transmitter blocks may easily be adapted to provide the required reference outputs. Gates 35 23 and 25 may be external.

[0058] It should further be appreciated that reference drivers 14 and 16 could be adapted to produce output voltages different from voltage levels used by transmitters 12 to represent HI and LO signals. For example, drivers 14 and 16 could be adapted to produce generalized low and high threshold voltage levels used to detect HI and LO signals. Thus, the margin or hysteresis voltages used by a receiver could be set at the transmitter source.

40 [0059] Finally, it will be understood that the invention is not limited to the embodiments described herein which are merely illustrative of a preferred embodiment of carrying out the invention, and which are susceptible to modification of form, arrangement of parts, steps, details and order of operation. The invention, rather, is intended to encompass all such modifications within its scope, as defined by the claims.

45

Claims

1. A signal transmitter block formed as part of an integrated circuit, said transmitter block for transmitting digital signals to a receiver, said block comprising:

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a plurality of signal drivers, each for generating output voltages at a signal driver output that when measured relative to a ground point on said integrated circuit are representative of digital HI and LO signals;

55

a first reference driver, for generating at a first reference output, one of:

- a) an output voltage that when measured relative to said ground point, corresponds to a voltage representative of a digital HI signal; and
- b) an output voltage that when measured relative to said ground point corresponds to a voltage repre-

- sentative of a digital LO signal;
- 5 said first reference driver and said signal drivers electrically interconnected to said ground point on said integrated circuit block,
- 10 said ground point interconnected through an impedance on said integrated circuit block to a system ground connection for said integrated circuit, so that current flowing from and to said system ground connection through said ground point to said signal drivers and
- 15 said first reference driver flows through said impedance.
2. The transmitter block of claim 1, wherein said impedance is attributable to a package impedance of said integrated circuit.
- 15 3. The transmitter block of claim 1 or claim 2, wherein
- 20 said signal drivers and said first reference driver are adapted for interconnection to a clock source;
- 20 said signal drivers are adapted to be driven to produce outputs representative of inputs at transitions of said clock source; and
- 25 wherein said impedance produces identical noise signals relative to said system ground connection at said signal driver outputs and said first reference output as a result of currents flowing at said transitions.
- 25 4. The transmitter block of claim 1, 2 or 3, further comprising
- 30 a second reference driver, for generating at a second reference output, the other one of
- 30 a) an output voltage that when measured relative to said ground point, corresponds to a voltage representative of a digital HI signal; and
- 30 b) an output voltage that when measured relative to said ground point corresponds to a voltage representative of a digital LO signal;
- 35 said second reference driver interconnected to said ground point on said integrated circuit so that current flowing from and to said ground connection through said ground point to said second reference driver also flows through said impedance.
- 40 5. The transmitter block of claim 4, wherein said second reference driver is adapted for interconnection to a clock source, and wherein said impedance produces noise signals at said second reference output identical to noise signals at said first reference output, as a result of currents flowing at said transitions.
- 45 6. The transmitter block of any preceding claim, wherein said plurality of signal drivers comprises less than sixteen signal drivers, geometrically proximate on said integrated circuit.
- 45 7. The transmitter block of any one of claims 1 to 5, wherein said plurality of signal drivers comprises less than eight signal drivers, geometrically proximate on said integrated circuit.
- 50 8. A digital signal receiver block having receiver block outputs for generating digital HI and LO signals, said block comprising:
- 50 a plurality of comparators, each having
- 55 a signal input for receiving a voltage signal representative of one of a digital HI signal and LO signal and a noise signal;
- 55 an output interconnected with one of said receiver block outputs;
- 55 a first reference input for receiving a reference voltage signal including a signal indicative of a digital HI signal,

and a noise signal;

wherein said first reference inputs of said plurality of comparators are interconnected so that each of said first reference inputs receives the same reference voltage signal;

5 each said comparator adapted to produce at its output a signal representative of a digital HI signal when a voltage at its signal input exceeds a threshold voltage derived from a reference voltage at its first reference input.

9. The receiver block of claim 8, wherein said threshold voltage equals a reference voltage at its first reference input less a voltage representative of a noise margin.

10. The receiver block of claim 8 or claim 9, further comprising

a clock input;

15 a latch interconnected with said clock input and with each output of said plurality of comparators,

said latch adapted to latch said comparator outputs upon a transition at said clock input.

11. The receiver block of claims 8, 9 or 10, wherein each of said comparators further comprises

20 a second reference input for receiving a reference voltage signal including a signal indicative of a high threshold voltage of a signal representative of a digital LO signal, and a noise signal;

25 wherein said second reference inputs of said plurality of comparators are interconnected so that each of said second reference inputs receives the same reference voltage signal; and

each of said comparators is adapted to produce at its output a signal representative of a digital LO signal when a voltage at its signal input is less than a threshold voltage derived from a reference voltage at its second reference input.

30 12. A digital signal receiver block having receiver block outputs for generating digital HI and LO signals, said block comprising:

35 a plurality of comparators, each having

a signal input for receiving a voltage signal representative of one of a digital HI signal and LO signal and a noise signal;

40 an output interconnected with one of said receiver block outputs,

a first reference input for receiving a reference voltage signal including a signal indicative of a digital LO signal, and a noise signal;

45 wherein said first reference inputs of said plurality of comparators are interconnected so that each of said reference inputs receives the same reference voltage signal; and

each of said comparators is adapted to produce at its output a signal representative of a digital LO signal when a voltage at its signal input is less than a threshold voltage derived from a reference voltage at its first reference input.

50 13. The receiver block of claim 12, further comprising

a clock input;

55 a latch interconnected with said clock input and with each output of said plurality of comparators,

said latch adapted to latch said comparator outputs upon a transition at said clock input.

14. The receiver block of claim 12 or 13, wherein each of said comparators further comprises

a second reference input for receiving a reference voltage signal including a signal indicative of a digital HI signal, and a noise signal;

5 wherein said second reference inputs of said plurality of comparators are interconnected so that each of said second reference inputs receives the same reference voltage signal; and

10 each of said comparators is adapted to produce at its output a signal representative of a digital HI signal when a voltage at its signal input exceeds a threshold voltage derived from a reference voltage at its second reference input.

15 15. The receiver block of claim 14, wherein each of said comparators is adapted to produce an error signal when a voltage at said signal input of said comparator is less than said threshold voltage derived from a reference voltage at its second reference input and exceeds said threshold voltage derived from a reference voltage at its first reference input.

20 16. The receiver block of any one of claims 12 to 15, wherein said threshold voltage equals a reference voltage at said first reference input plus a determined noise margin voltage.

25 17. A method of transmitting and receiving a plurality of signals representative of digital HI and LO signals from a transmitter to a receiver comprising the steps of

concurrently transmitting said plurality of signals, each having a voltage level representative of one of a digital HI and LO signal and a noise signal from a transmitter to a receiver;

25 transmitting a reference signal comprised of a signal having a voltage level representative of a HI signal and a noise signal to said receiver;

receiving said plurality of signals and said reference signal at said receiver;

30 comparing said reference signal to each of said plurality of signals;

outputting a signal representative of a digital HI signal at said receiver, for each of said plurality of signals that exceeds a threshold voltage derived from said reference signal.

35 18. The method of claim 17, wherein the steps are synchronized by a clock signal at said transmitter and said receiver.

19. A signal transmitter block for transmitting digital signals to a receiver, said block comprising:

40 means for transmitting a plurality of output signals, each output signal comprised of a voltage signal representative of digital HI and LO signals and noise;

means for transmitting a reference signal, representative of said noise and a determined one of

- 45 a) a signal having a voltage level representative of a digital HI signal; and
b) a signal having a voltage level representative of a digital LO signal.

20. A receiver comprising:

50 means to receive a plurality of received signals each received signal comprised of a voltage signal representative of digital HI and LO signals and noise;

means to receive a reference signal representative of said noise and a determined one of

- 55 a) a signal having a voltage level representative of a digital HI signal; and
b) a signal having a voltage level representative of a digital LO signal.

means to compare each of said plurality of received signals to said reference signal to determine whether each of said plurality of signals comprises a voltage signal representative of a digital HI signal, or a voltage

signal representative of a digital LO signal.

21. In combination,

5 a signal transmitter block formed as part of an integrated circuit, said transmitter block for transmitting digital signals to a receiver, said block comprising:

10 a plurality of signal drivers, each for generating output voltages at a signal driver output, that when measured relative to a ground point on said integrated circuit are representative of digital HI and LO signals;

15 a first reference driver for generating at a first reference output an output voltage that when measured relative to said ground point corresponds to a voltage representative of a digital LO signal;

20 said first reference driver and said signal drivers electrically interconnected to said ground point on said integrated circuit block,

25 said ground point interconnected through an impedance on said integrated circuit block to a system ground connection for said integrated circuit, so that current flowing from and to said ground connection through said ground point to any and all of said signal drivers and said first reference driver flows through said impedance; and

30 a digital signal receiver block having receiver block outputs for generating digital HI and LO signals, said block comprising:

35 a plurality of comparators, each having

40 a signal input interconnected with one of said signal drivers outputs for receiving a voltage signal representative of one of a digital HI signal and LO signal and a noise signal;

45 an output interconnected with one of said receiver block outputs,

50 a first reference input interconnected with said first reference driver for receiving a reference voltage signal including a signal indicative of a digital LO signal, and a noise signal;

55 wherein said first reference inputs of said plurality of comparators are interconnected so that each of said first reference inputs receives the same reference voltage signal; and

each of said comparators is adapted to produce at its output a signal representative of a digital LO signal when a voltage at its signal input is less than a threshold voltage derived from said reference voltage at its first reference input.

22. A signal transmitter formed as part of an integrated circuit, said transmitter for transmitting digital signals to a receiver, said transmitter and said receiver interconnected with a system ground, said transmitter comprising:

45 a plurality of signal drivers, each for generating output voltages at a signal driver output, that when measured relative to a ground point on said integrated circuit are representative of digital HI and LO signals;

50 a first reference driver, for generating at a first reference output, an output voltage that when measured relative to said ground point, corresponds to a voltage representative of a digital LO signal and that when measured relative to said system ground comprises a noise signal indicative of a noise component in signals representative of digital LO signals.

23. A signal transmitter formed as part of an integrated circuit, said transmitter for transmitting digital signals to a receiver, said transmitter and said receiver interconnected with a system ground, said transmitter comprising:

55 a plurality of signal drivers, each for generating output voltages at a signal driver output, that when measured relative to a ground point on said integrated circuit are representative of digital HI and LO signals;

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a first reference driver, for generating at a first reference output, an output voltage that when measured relative to said ground point, corresponds to a voltage representative of a digital HI signal and that when measured relative to said system ground comprises a noise signal indicative of a noise component in signals representative of digital HI signals.

5

24. In combination,

a signal transmitter block for transmitting digital signals to a receiver, said block comprising:

10 a plurality of signal drivers, each for generating output voltages at a signal driver output, that when measured relative to a ground point on said integrated circuit are representative of digital HI and LO signals;

15 a first reference driver, for generating at a first reference output, an output voltage that when measured relative to said ground point corresponds to a voltage representative of a digital LO signal;

20 a digital signal receiver block having receiver block outputs for generating digital HI and LO signals, said block comprising:

25 a plurality of comparators, each having

30 a signal input interconnected with one of said signal drivers outputs for receiving a voltage signal representative of one of a digital HI signal and LO signal and a noise signal;

35 an output interconnected with one of said receiver block outputs,

a first reference input interconnected with said first reference driver for receiving a reference voltage signal including a signal indicative of a digital LO signal, and a noise signal;

40 wherein said first reference inputs of said plurality of comparators are interconnected so that each of said first reference inputs receives the same reference voltage signal; and

45 each of said comparators is adapted to produce at its output a signal representative of a digital LO signal when a voltage at its signal input is less than a threshold voltage derived from said reference voltage at its first reference input.

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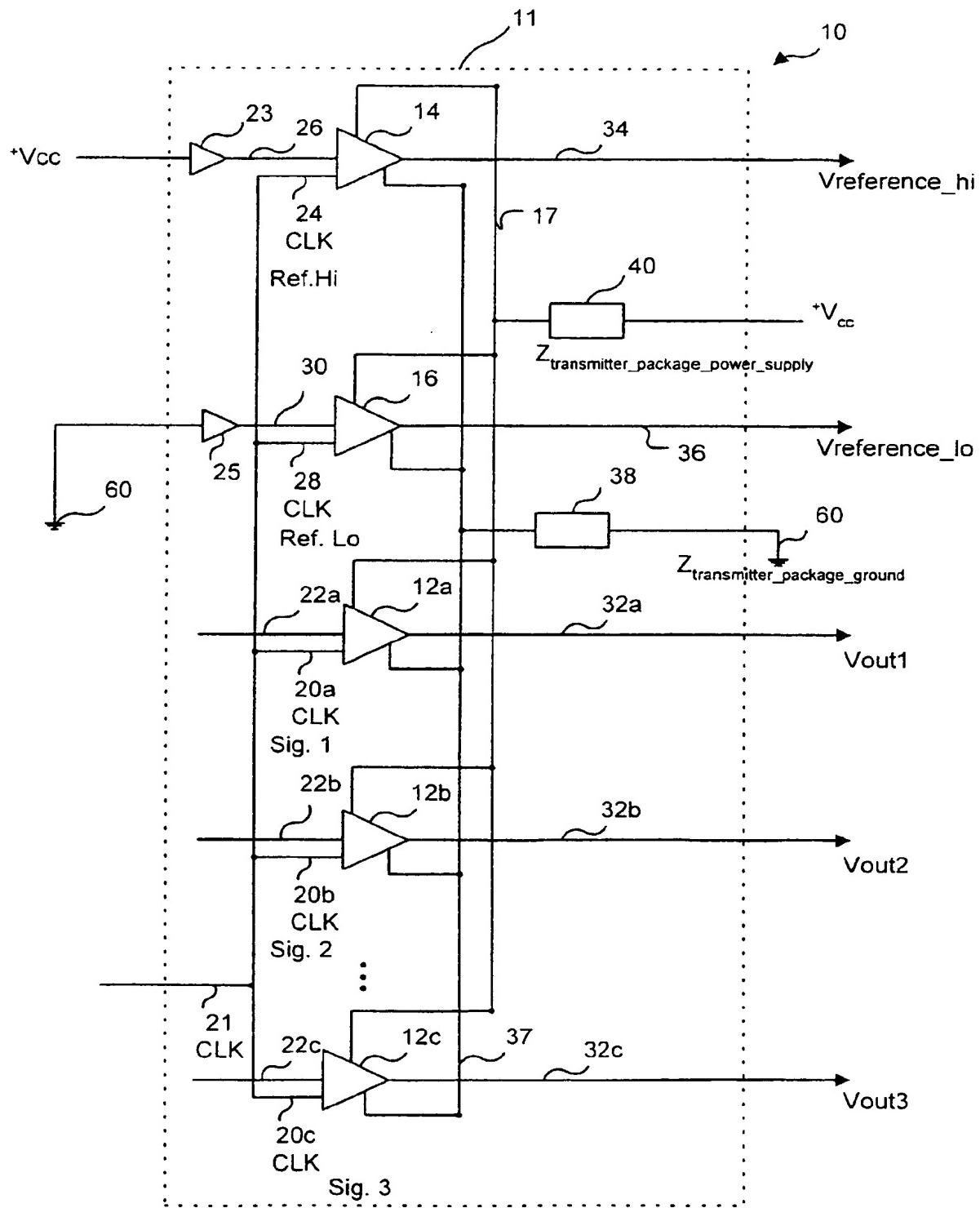


FIG. 1

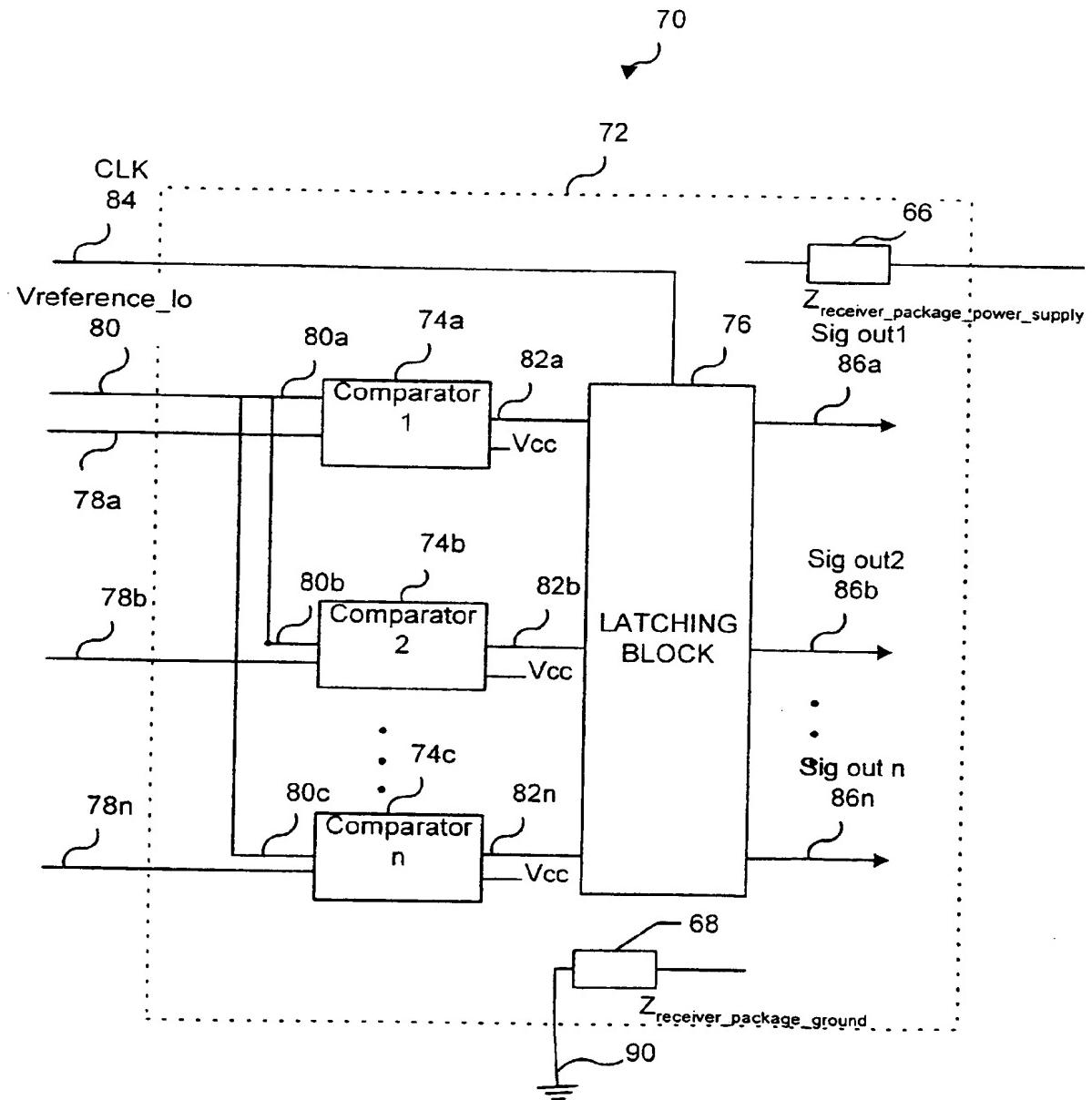


FIG. 2

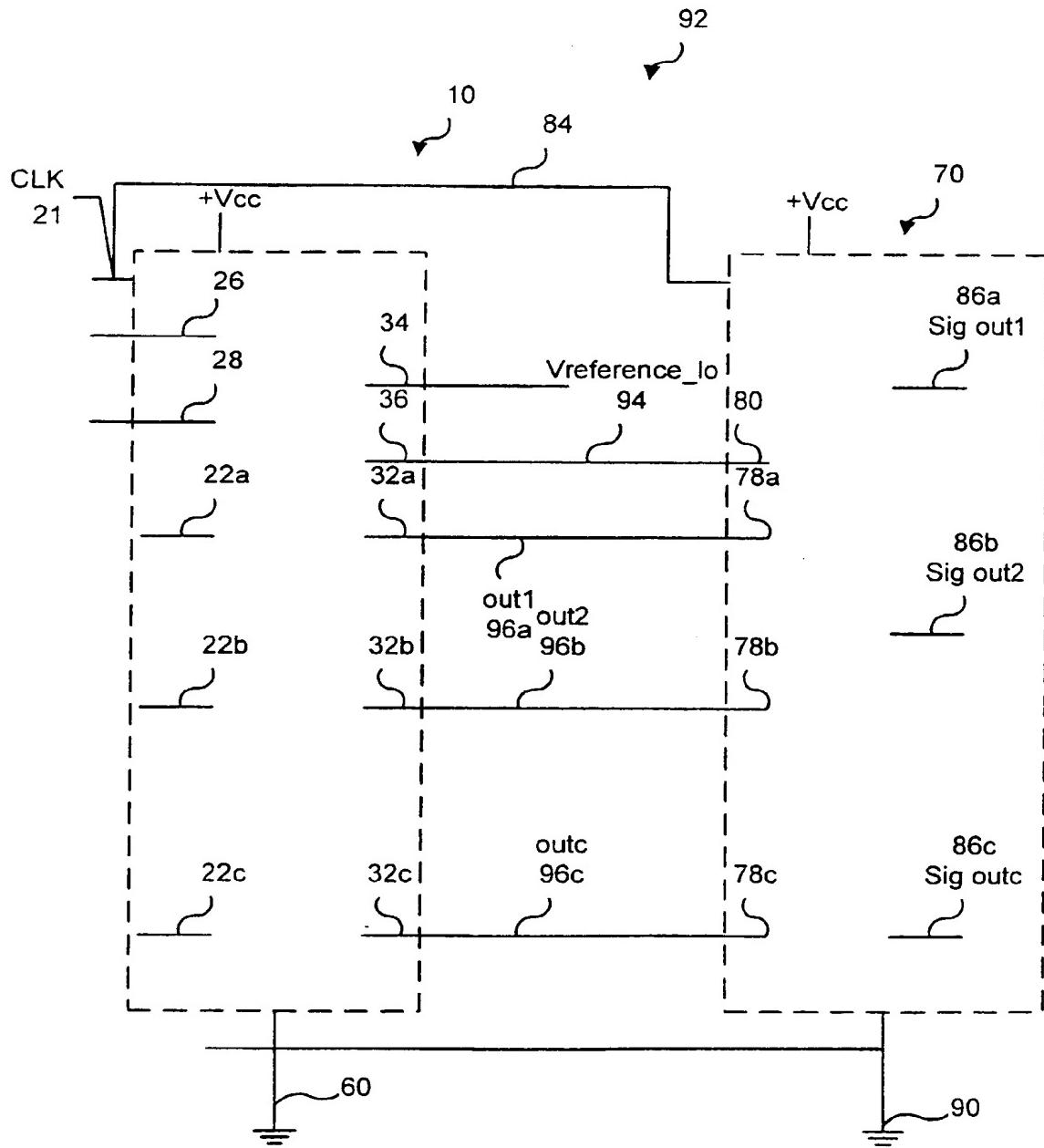


FIG. 3

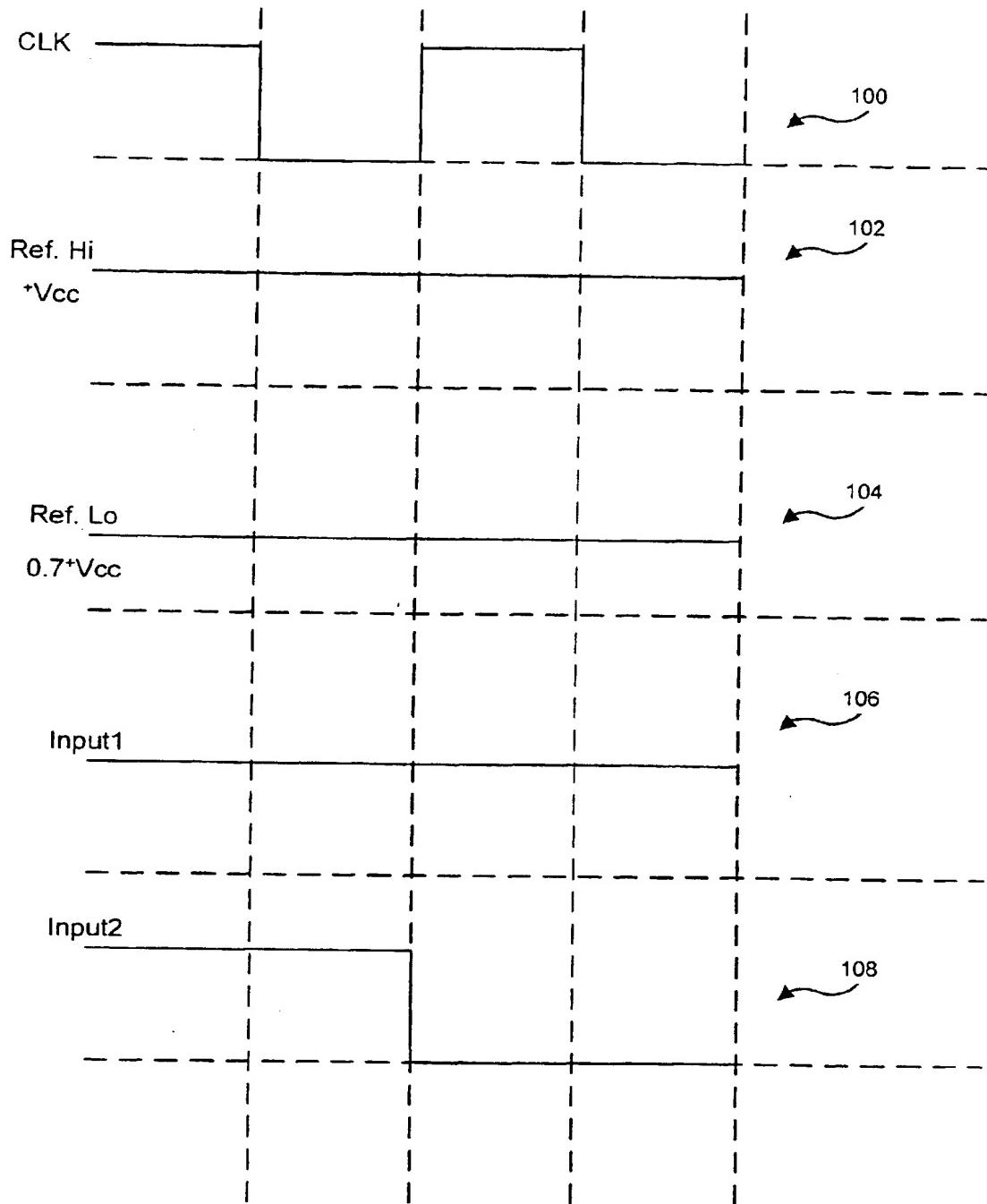


FIG. 4

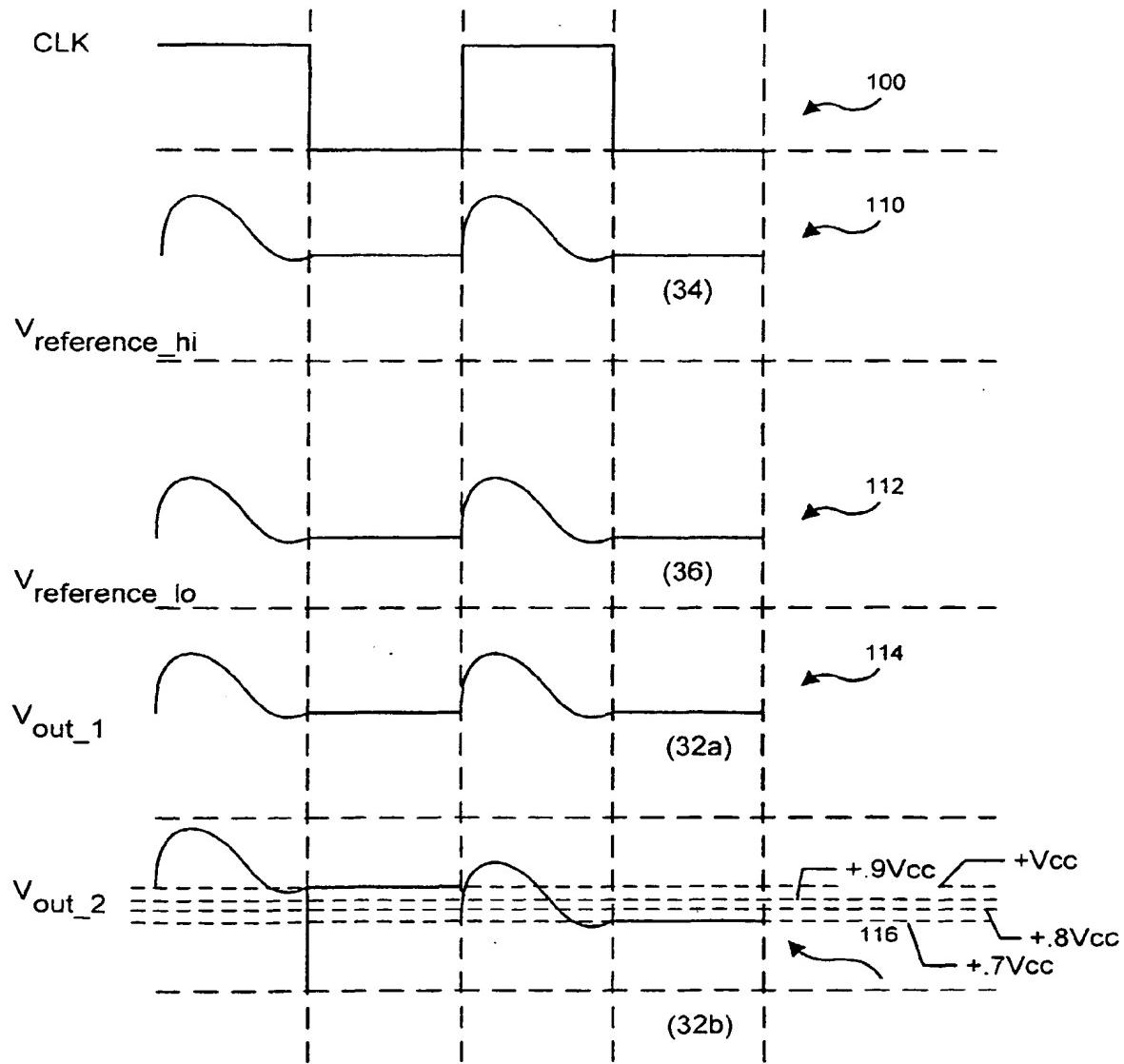


FIG. 5



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9742

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<p>The present search report has been drawn up for all claims</p> <table border="1"> <tr> <td>Place of search</td> <td>Date of completion of the search</td> <td>Examiner</td> </tr> <tr> <td>MUNICH</td> <td>14 March 2000</td> <td>Moll, P</td> </tr> </table>				Place of search	Date of completion of the search	Examiner	MUNICH	14 March 2000	Moll, P
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MUNICH	14 March 2000	Moll, P							
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons S : member of the same patent family, corresponding document</p>									

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